WBS 1.1.1 Pixel System

Sensors and Electronics

Module Design

- Sensors (WBS 1.1.1.2): Status and Issues
- On-Detector Electronics (WBS 1.1.1.3): Status and Issues

Prototype Results

- Testbeam results from pixel assemblies

Summary and Conclusions

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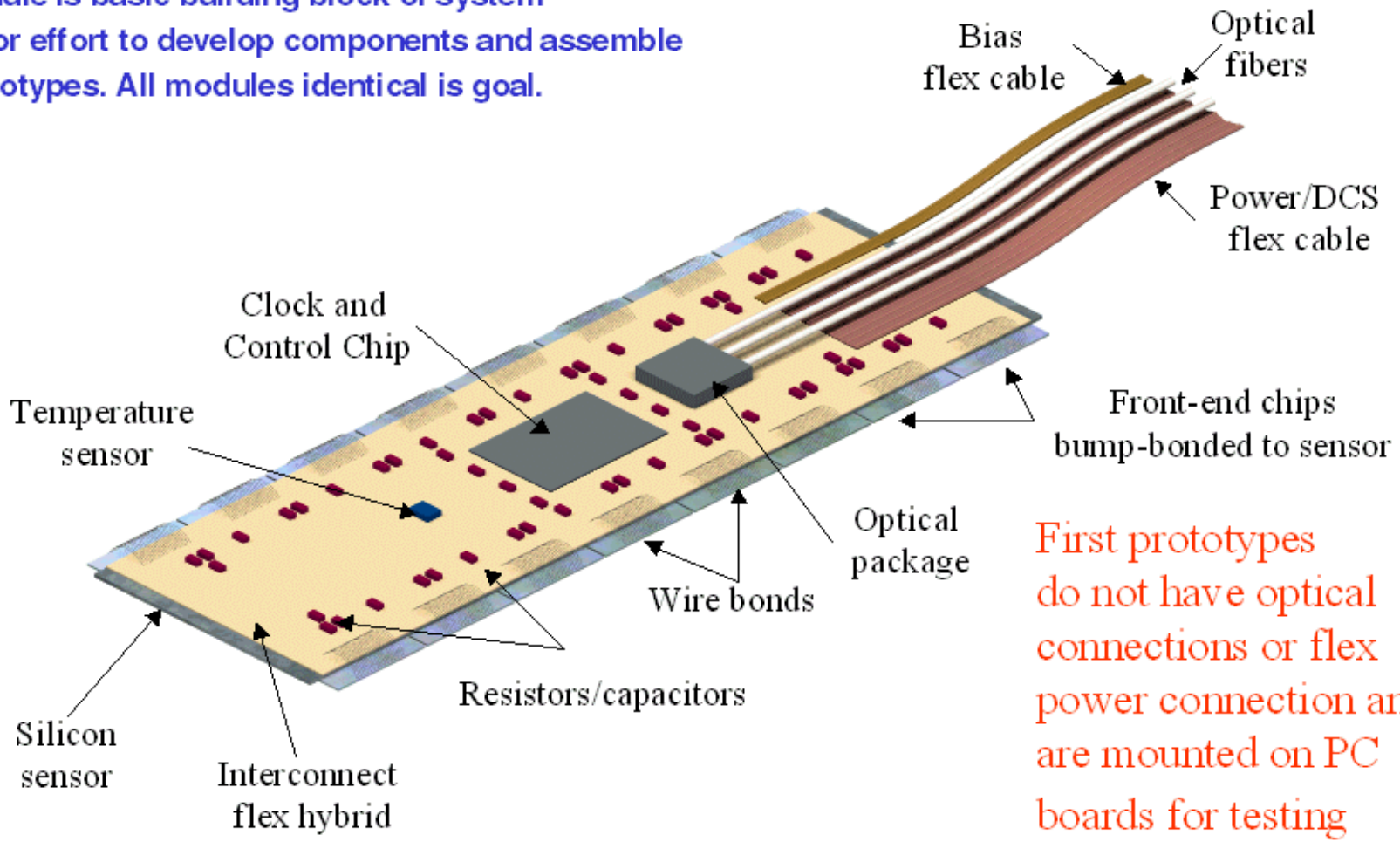
Basic Components of Pixel Tracker

Modules placed on a mechanical support/cooling structure:

- Silicon sensor with 16 FE chips, controller chip, power cable and opto-link

Module is basic building block of system
Major effort to develop components and assemble prototypes. All modules identical is goal.



First prototypes do not have optical connections or flex power connection and are mounted on PC boards for testing

- Present concept has optolink mounted on pigtail as part of cable harness.

Sensor Concepts

Basic requirement is operation after 10^{15} NIEL fluence:

- Requires partially depleted operation. Chosen n^+ pixels in n-bulk material as basic configuration (does require double-sided processing).
- Two isolation techniques have been studied for the n^+ pixel implants. First is conventional p-stop method. Second uses low-dose p implantation over the whole wafer (so-called p-spray). With p-spray technique, observe only bulk leakage in I/V curve after full dose (not true for p-stop), a bias grid can be used for wafer-scale testing, and no lithography between n^+ implants is needed.

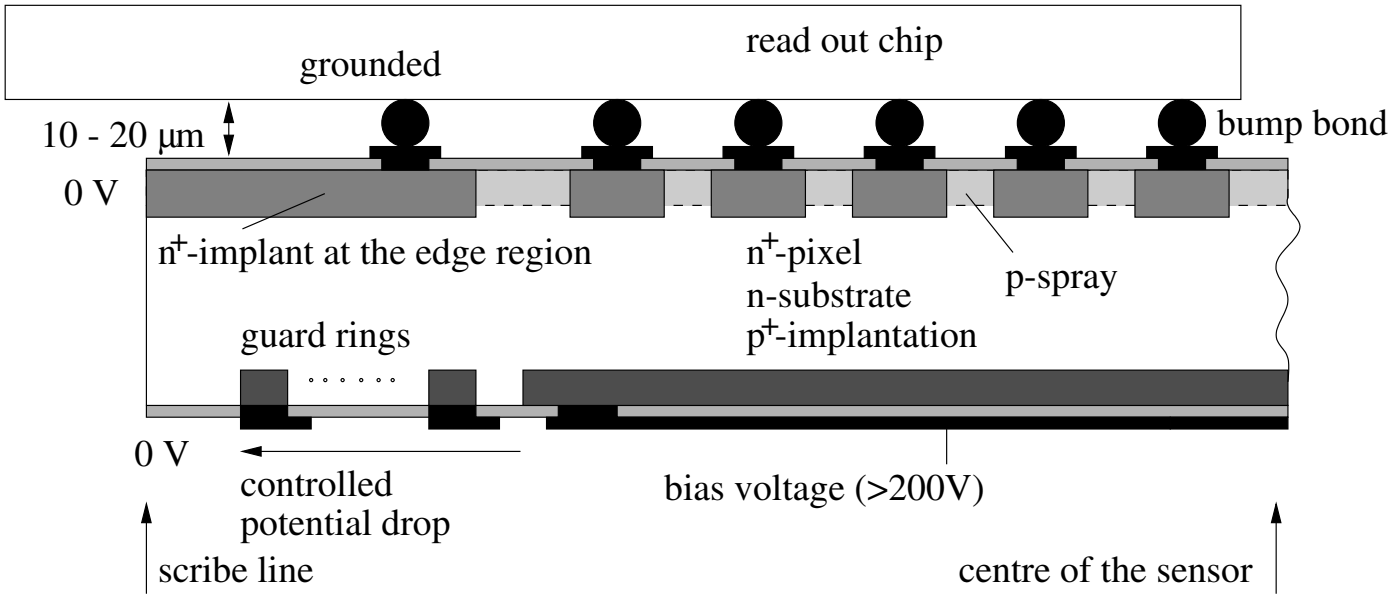
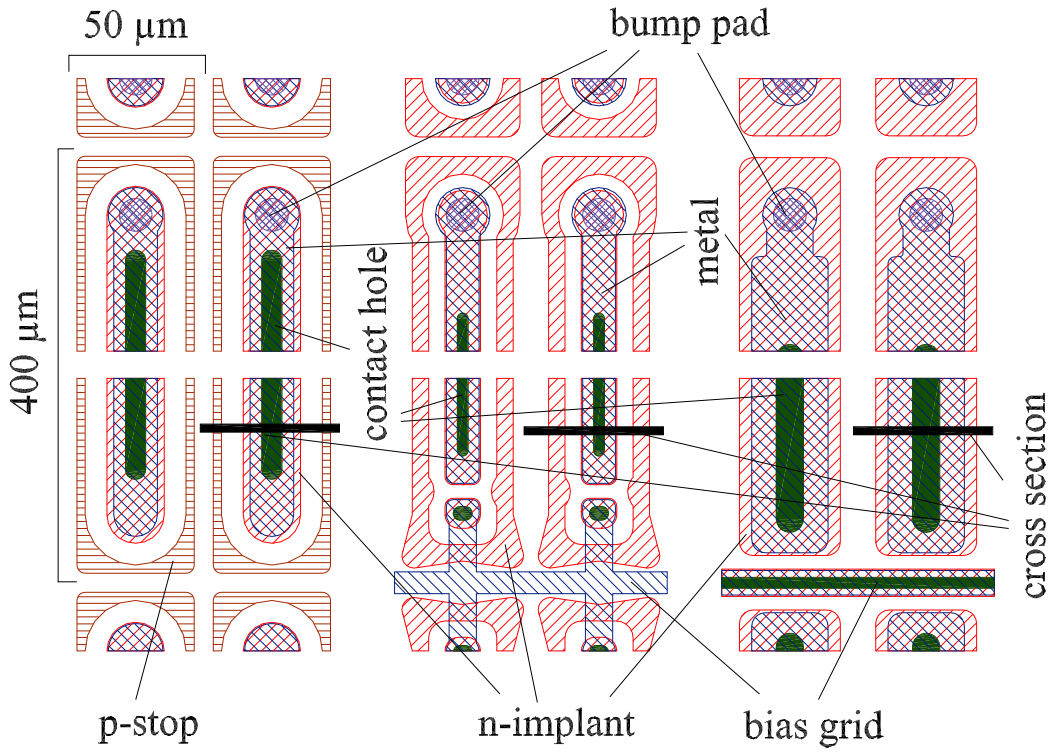


Diagram showing guard geometry near edges of module, designed to operate safely with bias voltages of beyond 700V.

Sensor Prototypes (Sensor 1)

Geometry of module:

- Design has an active region of 16.4 x 60.8mm, containing 46,080 pixels of 50μ x 400μ. The B-layer should use 61,440 50μ x 300μ pixels. The thickness will be 250μ in the outer layers, reduced to 200μ in the B-layer. An additional 1mm non-active region is used for the guard rings.
- Several designs were prototyped. Final designs are from Dortmund/MPI:



P-stop design had good charge collection and low capacitance, but had post-irradiation breakdown

Floating n-ring design had low capacitance but significant charge loss near ring.

Small gap design had higher capacitance, but otherwise excellent behavior.

Final Sensor Design (Sensor 2)

- Final design is based on small gap, and includes bias grid to allow testing (hold all pixel implants at ground for I/V characterization) and to keep unconnected pixels from floating to large potential in case of bump-bonding defects. It uses "moderated" p-spray to improve pre-rad breakdown voltage (better yield).
- Sensor 2 wafer layout has 3 module tiles ("no dot", "small dot", and "large dot" bias structures) and many test structures in 4" wafer:

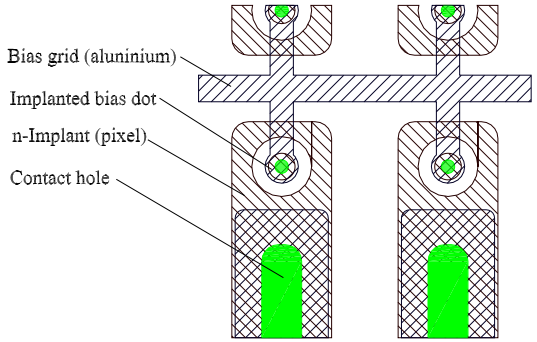
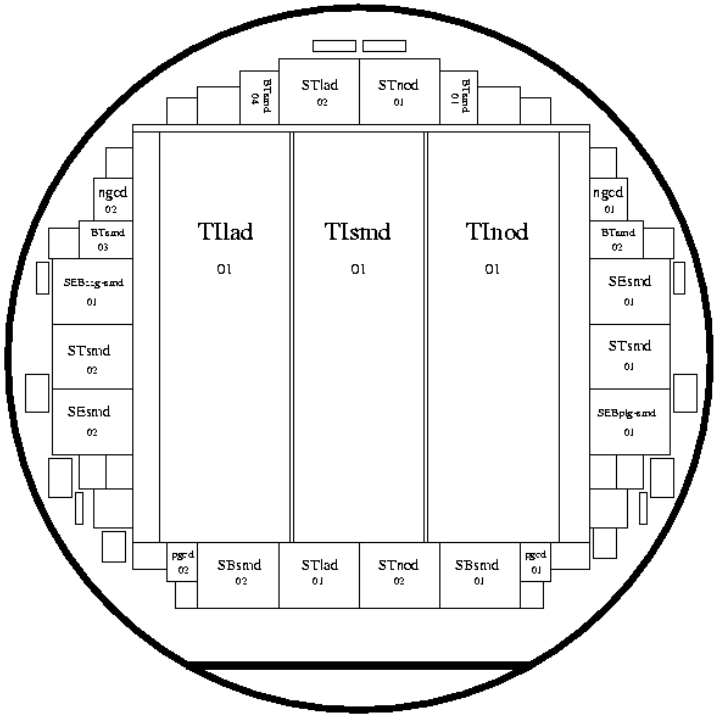
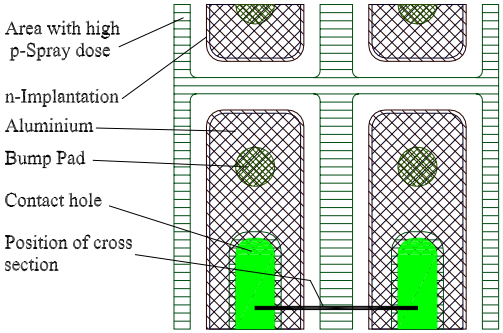
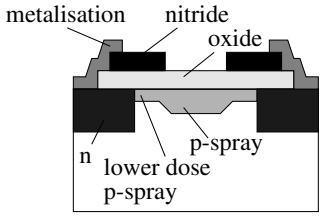


Fig. 10. Design detail of the bias grid in the second sensor prototype.



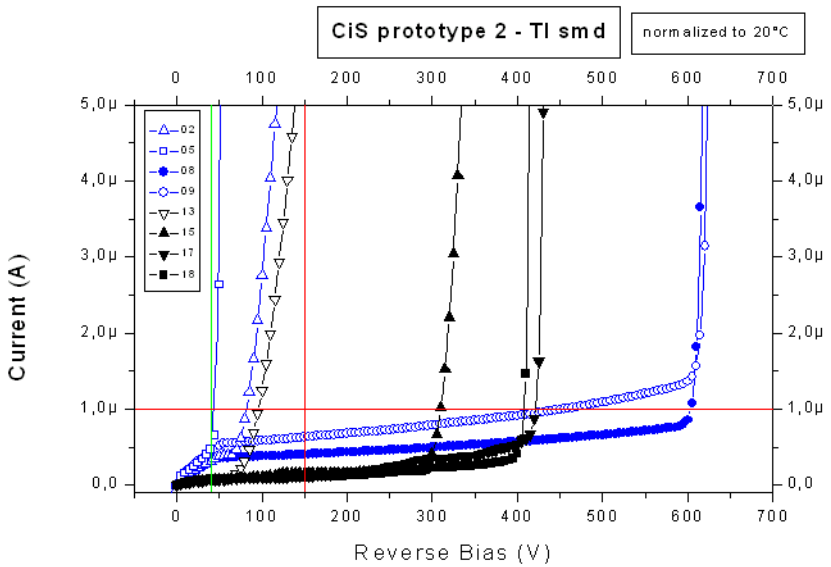


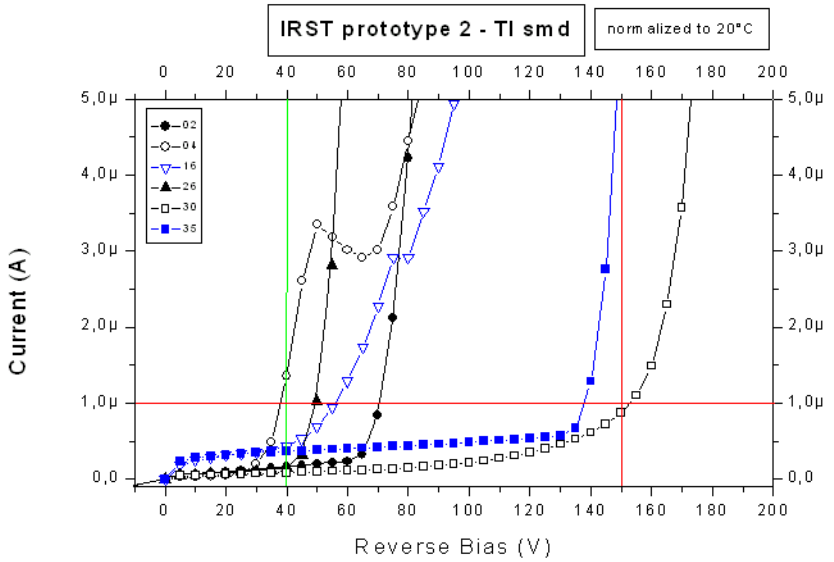


Prototype History:

- **Sensor 1 designs:** Initial designs from 1997 covering a wide range of concepts with CIS and Seiko. Extensively tested in the lab and testbeam in 1998, including irradiation of single chips and subsequent flip-chip to rad-soft electronics.
- **Sensor 1b designs:** Evolution of p-spray designs to include version very close to final production concept (SSGb). Only CIS was a vendor. Extensively tested in lab and beam in 1999. A second identical run (sensor 1c) was used to compare yield for standard and moderated p-spray.
- **Sensor 2 designs:** Emphasis on final wafer layout, significant orders to exercise vendors and allow us to build a large number of modules. Uses latest technology, including moderated p-spray and 50% of wafers oxygenated using ROSE recipe.
- **Oxygenation:** Technique involves diffusion into wafers for 16 hours at 1150 C in O atmosphere. Only useful when irradiation is predominantly charged particles (neutron damage un-affected). Two major effects (other properties unchanged):
- Modification of reverse annealing behavior by “saturating” the total reverse annealing. This gives about half depletion voltage for a fixed large dose. For B-layer, roughly doubles lifetime dose (ignoring trapping effects).
- Increase of reverse annealing time constant by about 4. This gives reduced effect of room temperature exposure on irradiated sensors, and considerably relaxes access scenarios. Largely understood in terms of defect phenomenology.

- Yield from CIS is presently marginal (about 70% per tile), but expected to improve. Second vendor (IRST) yield is not yet acceptable on tiles (low breakdown voltage), but single chips look OK. They are producing a second batch. Some sample I/V curves are shown below:





- These devices will be studied in the testbeam in the near future.
- Market Survey completed and Tender initiated according to CERN procurement rules. Three potential vendors for production (CIS, CSEM/IRST, SINTEF), plus additional Czech vendor under study (TESLA). ATLAS plans to use at least two of these vendors to reduce risk and meet production schedule.
- FDR (Dec 3 99) and PRR (Feb 2 00) successfully completed.

US Roles:

- There are four active testing sites in pixels (Dortmund, New Mexico, Prague, and Udine). Test procedures and acceptance criteria are defined in great detail.
- UNM has performed US share of wafer probing up to the present, and has necessary equipment set up. University of Oklahoma plans to assist once the production wafers begin to flow.

Next Steps and Remaining Issues:

- Complete evaluation of pre-production prototypes (sensor 2) from two vendors.
- Further irradiation studies must be performed. These include validation of moderated p-spray concept and oxygenated material benefits for pixel designs attached to real electronics.
- Critical concern is production ability of the vendors (traditional vendors either were not interested or were not qualified for pixel production). There are two issues: achieving and maintaining an acceptable yield (something in the range of 70% or more per tile), and delivering serial production quantities.
- Because of concerns about these issues, we will push ahead with pre-production by the middle of this calendar year .

Deliverables:

US Responsibilities include the following:

- Participate in the design and testing of the sensors.
- Contribute roughly 20% towards the common procurement of prototype and production sensor wafers.
- The estimate for the number of production wafers is 1200, including preliminary estimates for fabrication yield and module assembly yield.
- ATLAS evaluating acceptance criteria for production wafers, but likely to require at least two good tiles per wafer, so low yield risk is largely carried by vendors.
- Present cost estimate for production is based on recent purchases. Will have vendor responses to Tender for the September Baseline Review.
- Present US Production Cost Estimate (preliminary) is:

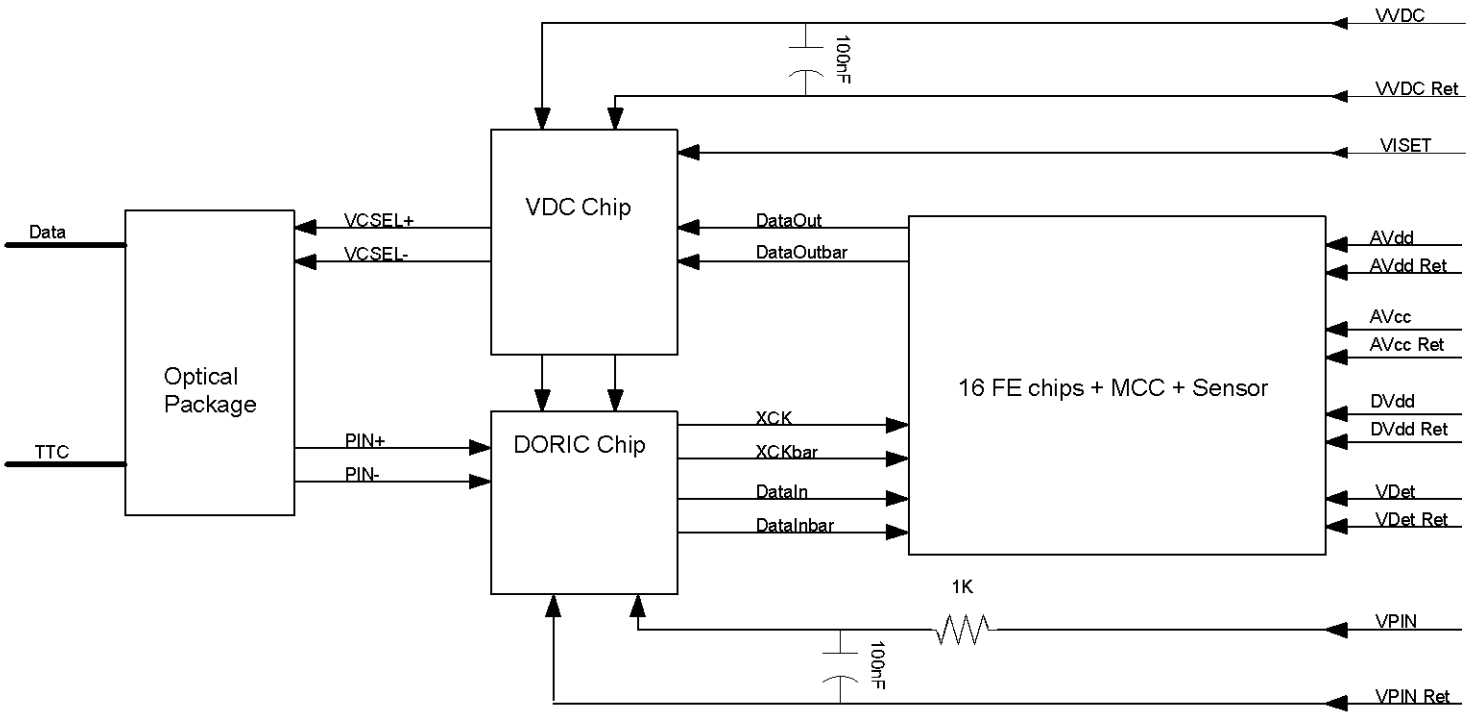
WBS Number	Description	Base Cost	Cont Cost (k$)	Cont %	Total Cost	EDIA Labor	Mfg Labor	EDIA Matls	Mfg Matls	FTEs Project	FTEs Other
1.1.1.2.3	Production	581	131	22	712	0	21	0	560	1.1	0.0
1.1.1.2.3.1	Layers 1/2 and Disks and B-layer	581	131	22	712	0	21	0	560	1.1	0.0
1.1.1.2.3.1.1	Preproduction	73	0	0	73	0	0	0	73	0.0	0.0
1.1.1.2.3.1.2	Production	480	125	26	605	0	0	0	480	0.0	0.0
1.1.1.2.3.1.3	Testing	29	6	20	34	0	21	0	8	1.1	0.0

On-Detector Electronics Concepts

System Design:

- **Pixel Array (Bonn/CPPM/LBL):** FE chip of 7.4 x 11.0mm die size with 7.2 x 8.0mm active area. The chip includes a serial command decoder, Clock, LVL1, and Sync timing inputs, and serial 40 Mbit/s data output. The set of hits associated with a particular crossing is “requested” by sending LVL1 signal with correct latency. FE chip then transmits corresponding digital hits autonomously.
- **Module Controller (Genova):** Collects data from 16 FE chips and implements a silicon event builder. Performs basic integrity checks and formats data, also implements module level command/control. The 16 FE chips on module connect to MCC in star topology to eliminate bottlenecks and increase fault tolerance.
- **Opto-link (OSU/Siegen/Wuppertal):** Multiplexed clock/control sent over 40 Mbit/s link to module, data is returned on one or two 80 Mbit/s data links. Transmitters are VCSELs, receivers are epitaxial Si PIN diodes. Basic link is 5x5x1.5mm package, and there are two additional small optolink chips with LVDS interfaces. The fibers are rad-hard silica core multi-mode fiber from Fujikura.
- **Power Distribution:** Significant ceramic decoupling on module. Flex power tape used to reach services patchpanels on cryostat wall (1.5m) followed by Al round cable to transition on back of calorimeter, then conventional cables to USA15 cavern. Additional filtering and protection on intermediate patch panels.

Summarize all connections required for module operation:



- There are six power supply voltages with their separate returns, and one control voltage that uses VVDCRet as a reference.
- VVDC powers both the DORIC and the VDC, and VPIN may connect directly to the opto-package instead of routing through the DORIC.
- Present concept is that DORIC, VDC and their passive components, plus the Opto-package are placed on Pigtail. Interface requires three LVDS signal pairs.

Electronics Challenges and Requirements

Main challenges are in FE chips:

- Operate properly after total dose of 50 MRad (nominal ATLAS 10 year dose). Also cope with expected leakage currents from sensors of up to 50nA per pixel. For the B-layer, this corresponds to a lifetime of about 2 years at design luminosity.
- Operate with low noise occupancy (below 10^{-6} hits/pixel/crossing) at thresholds of about 3Ke with good enough timewalk to have an “in-time” threshold of about 4Ke (hit appears at output of discriminator within 20ns of expected time). This requires a small threshold dispersion (about 300e) and low noise (about 300e).
- Associate all hits uniquely with a given 25ns beam crossing. Contributions to this timing come from timewalk in the preamp/discriminator, digital timing on FE chip, clock distribution on module, and relative timing of different modules.
- Meet specifications with nominal analog power of 40μW/channel and nominal total power for FE chip of 200mW (worst case budget is 70μW and 350mW).

Status of MCC chip:

- First version fabricated by Genova in AMS technology. Chip is roughly 70 mm^2, and 400K transistors. Other than a few very minor errors, it works well.
- Second generation now under design, with final system design, in DMILL process. Biggest concern is die size (may be quite large) and yield.

Pixel Opto-links:

- All AC signals (clock/commands/data) are transmitted optically to modules:
- **Receiver:** Fiber output is converted using an epitaxial Silicon PIN diode. The output (small current signal) is sent to the DORIC chip, which receives the 40 MHz crossing clock and a bi-phase mark encoded command stream as a single 40 Mbit/s serial stream. It uses a delay-locked loop to extract the clock (providing a high quality 50% duty-cycle clock) and decode the command stream. Note the command stream includes the synchronous LVL1 trigger commands, plus other synchronous commands, and slow configuration commands. An LVDS electrical interface is used to the MCC chip.
- **Driver:** The VDC chip converts LVDS data output streams from the MCC into current pulses suitable for driving the VCSELs chosen for data transmission. For pixel applications, the outer layers plan to use a single 80 Mbit/s output stream (provides roughly a factor 4 of safety), and the B-layer will use two 80 Mbit/s data streams. The format is NRZ, so the 80 Mbit/s link consists of sending a bit on each 40 MHz clock edge. The VCSEL drive current is adjustable using a remotely-controlled voltage. This allows in situ I/L curves, and also periodic operation at high bias to force rapid annealing of radiation damage.
- SCT groups (RAL/Oxford collaboration) have designed and produced two basic chips in pure bipolar AMS design. They work well, but are not likely to withstand pixel doses. For this reason, pixels began a conversion to rad-hard CMOS.

Status of DORIC-p and VDC-p:

- OSU converted design from AMS bipolar to DMILL CMOS, and simulated at schematic level. Siegen did layout, further simulations. Chips included in FE-D submission, and now under test. Several errors found in DORIC-p, which are still under study. Another iteration will be made before irradiation testing is possible.

Irradiation issues:

- Collaborative effort of SCT and pixels (Wuppertal from pixels) have performed systematic irradiation studies of optical fibers and opto-elements (PINs and VCSELs) up to pixel fluences. Results show no significant risks, provided PIN is operated with adequate bias voltage (up to about 7V), and provided VCSELs are operated with sufficient bias current (up to about 20mA).
- Only known issue at this time is single event upsets caused by interactions in the very thin epitaxial layer of the PIN diode. Further irradiations at PSI this Spring will clarify the magnitude of this effect, but it should be only an inconvenience. Specs for link pre-rad is BER of 10^{-12}, and post-rad is BER of as high as 10^{-9}. This should be easily achievable, but needs more complete system testing.
- Pixels has recently significantly upgraded the MCC command set to be highly fault tolerant. Critical commands (particularly LVL1) are successfully decoded under any single bit error, and are only mis-interpreted under double bit error.
- Remaining issue is proof of rad-hardness of opto-link electronics.

Power Distribution:

- ATLAS ID has chosen to operate detectors by placing all power supplies in USA15 (or US15) to allow use of standard commercial components.
- Major disadvantage is very long (up to 140m) cable runs required. Careful attention to engineering/prototyping of the power distribution system needed!

Concepts include:

- Single point grounding inside tracking volume with floating power supplies.
- Treatment of supply/return for supplies as low-impedance transmission lines (broad-side coupled pairs on Flex cables, twisted pair in conventional cables).
- Filtering (common-mode chokes and large capacitors) at PP3 to isolate detector from pickup going from USA15 to detector. Transient protection at PP1 to isolate modules from voltage surges that could kill electronics.
- Global (entrance level) decoupling with 0805 high density ceramics, and local (chip level) decoupling with 0402 high density ceramics on Flex hybrid. All digital and analog supplies are filtered. Material and envelope requirements are strict.
- Flex components are selected. Radiation testing will begin this Spring at CERN PS. Not yet clear whether design is adequate (noise/grounding/stability, etc.)
- Major issue is full system-level prototyping to validate concepts and performance. This requires working modules, cable prototypes, and noisy environments.

FE Electronics Prototypes

Several generations of prototypes have been built:

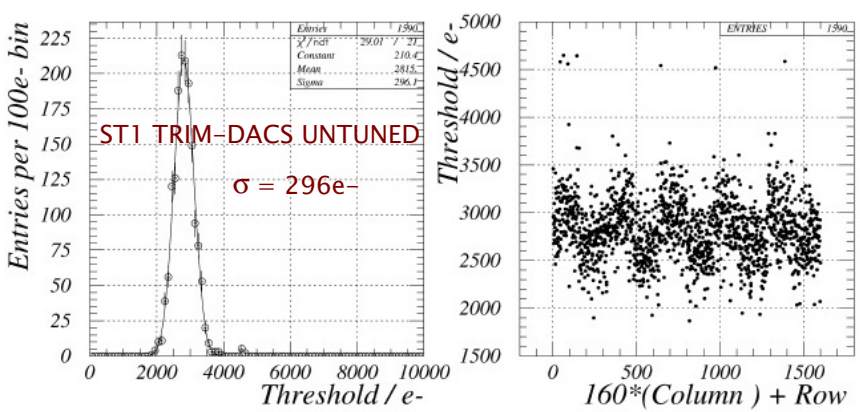
- First “proof of principle” chips were built in 96.
- First realistic prototypes were designed in two parallel efforts in 97/98, producing a rad-soft HP prototype (FE-B) and a rad-soft AMS prototype (FE-A/FE-C). These were 18 column, 160 row chips with 50μ x 400μ pixels.
- Prototypes of critical elements made in both rad-hard processes (TEMIC DMILL and Honeywell SOI) to study performance and radiation hardness.
- Ongoing activity focusses on common design DMILL chip (FE-D), and common design Honeywell chip (FE-H).

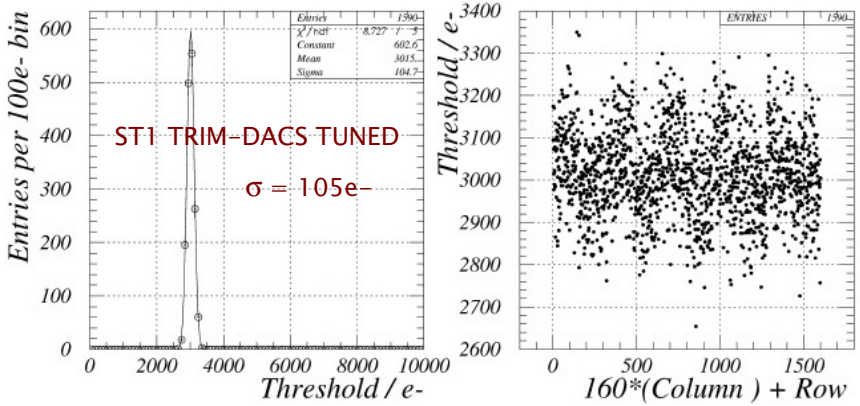
Features of final FE design:

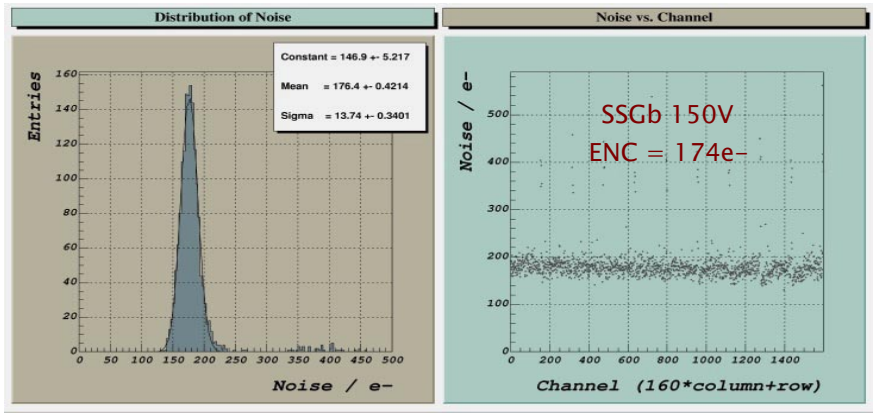
- Preamplifier provides excellent leakage current tolerance and relatively linear time-over-threshold (TOT) behavior via feedback bias adjustment.
- Discriminator is AC-coupled, and includes 3-bit trim DAC for threshold vernier.
- Readout architecture uses distributed 7-bit timestamp bus, and leading-edge plus trailing-edge latches in each pixel to define times of LE and TE.
- Asynchronous data push architecture used to get data into buffers at the bottom of the chip, where they are stored for the L1 latency, after which they are flagged for readout or deleted. Chip transmits Trigger/Row/Column/TOT for each hit.

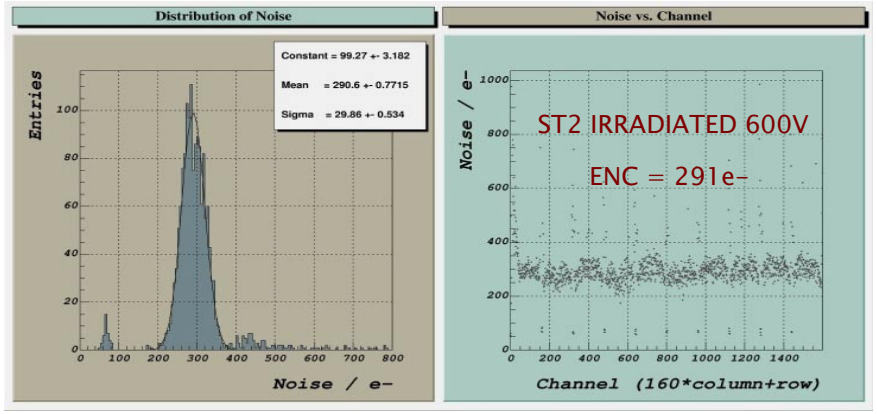
Lab Measurements using Rad-soft Prototypes

Examples of threshold and noise behavior in single chips:



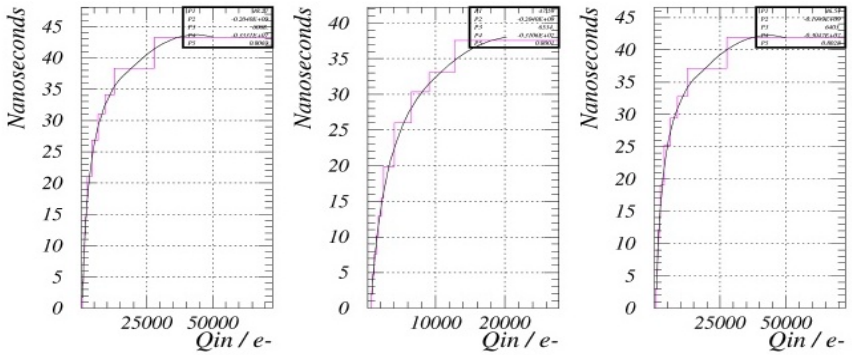




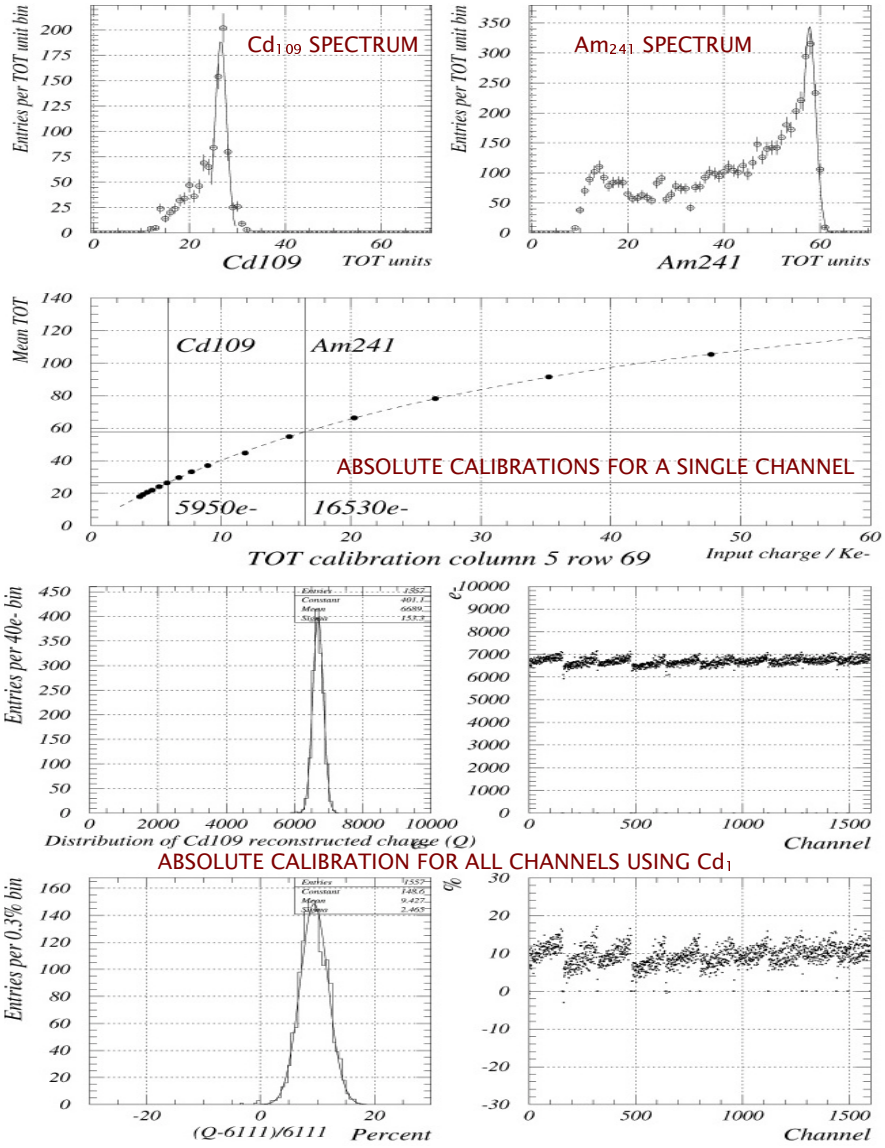


- Using individual Trim DACs, manage to achieve excellent dispersions.
- Measured noise is quite good, even for small-gap design pre-rad, and noise still remains acceptable after irradiation (reduced shaping time and parallel noise from leakage current itself both increase noise).

Examples of timing and charge measurements:

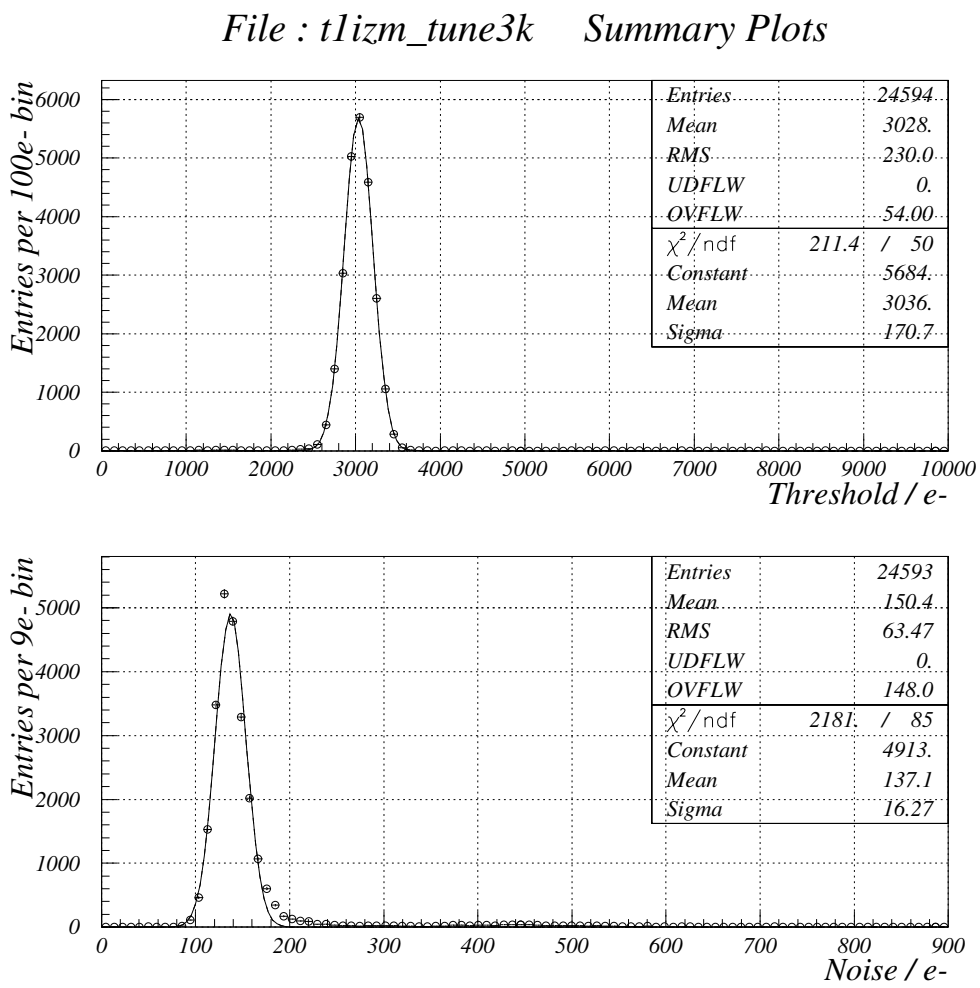


- Timing performance at large charge is excellent, and timewalk is acceptable.
- Charge measurement is high quality, but requires individual calibrations. Uniformity of internal calibration is good.



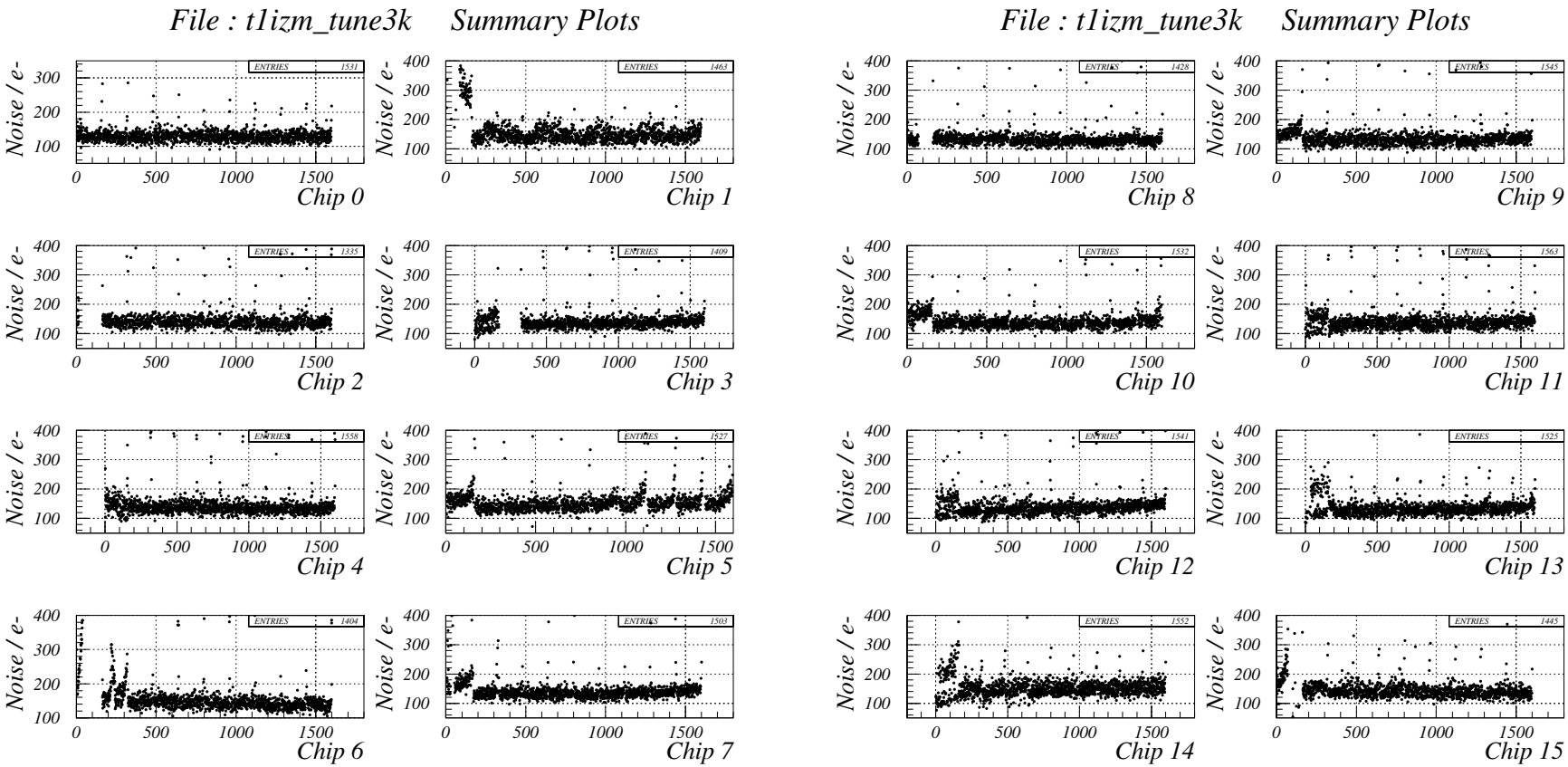
Examples of Module Results:

Bare Module (FE chips wire-bonded to PC board):



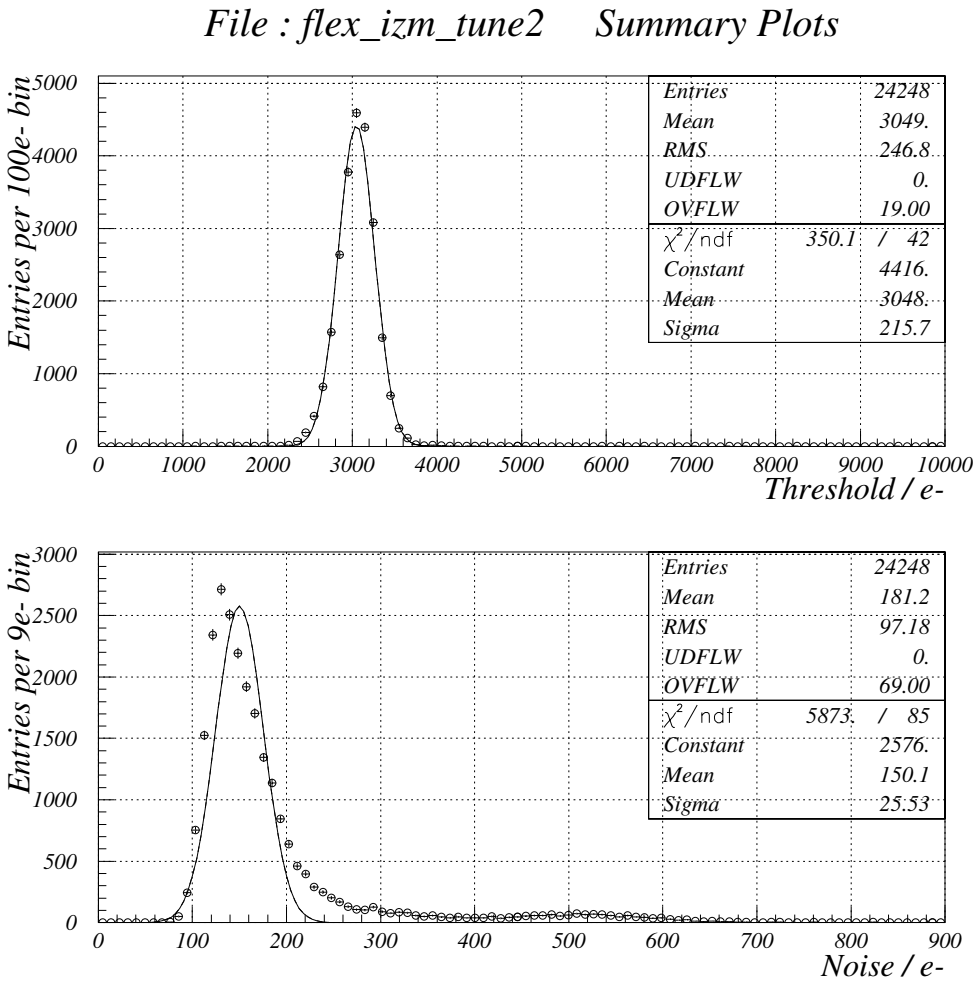
- Module has excellent threshold and noise behavior. For FE-B module should be only 16x1600 = 25600 good channels. Dead channels here are apparently all from bump-bonding problems (shorts).
- Threshold dispersion (230e) and noise (150e) for whole module are about same as for single chips.
- Module was operated in self-trigger mode at 70 KHz with excellent performance.

Plots of noise in each chip versus pixel number:



- Column 0 has longer pixels, plus most bumping defects (handling problem).
- This particular prototype comes close to meeting real ATLAS requirements for a module, although it is a rad-soft version.

Performance of best Flex module is not as good:



- Threshold dispersion is the same as for bare module.
- Noise distribution has a long tail. The origin of these noisy channels in this module is not clear.
- These results are from Spring 99, and have not been improved due to subsequent bumping problems with IZM which are still under study.

- Many impressive results from first prototype modules, but much larger statistics needed to check whether high quality modules can be built in a reproducible manner. Lab and testbeam characterization ability is now well-developed.

Radiation Hard Strategy

Pursue essentially identical designs with two vendors:

- **TEMIC/DMILL:** Began first work on FE-D in Summer of 98. Chip was submitted to TEMIC on Aug 10 99. Design contains some "simplifications" in digital readout from FE-B design to fit into DMILL constraints, as well as some improvements. Performance targeted at outer layers, with 400μ pixel and 24 EOC buffers per column pair. Readout performance should be adequate for operation at 10^{34}.
- Comments: CMOS density relatively low, especially for NMOS, and only two metal process. This forced design to make compromises. Have made minimal, but significant use of bipolars in FE-D. Barely succeeded in fitting necessary circuitry into available footprints. Concerns about radiation hardness for pixels.
- **Honeywell/SOI:** Began serious work on FE-H in Fall 99. At this time, only LBL and CERN had TAA agreements in place to do design. In addition, Honeywell was in process of revising Layout Rules, which caused significant delays. A number of minor improvements relative to FE-D, taking advantage of better device density and third metal layer. Design should be more robust, and performance is targeted at B-layer as well (goal: 300μ pixel and 32 EOC buffers).
- Comments: Density and routing both good, and can eliminate some compromises, and perhaps reach 300μ pixel. Radiation hardness of individual devices seems excellent. Cost is higher, so yield must also be higher.

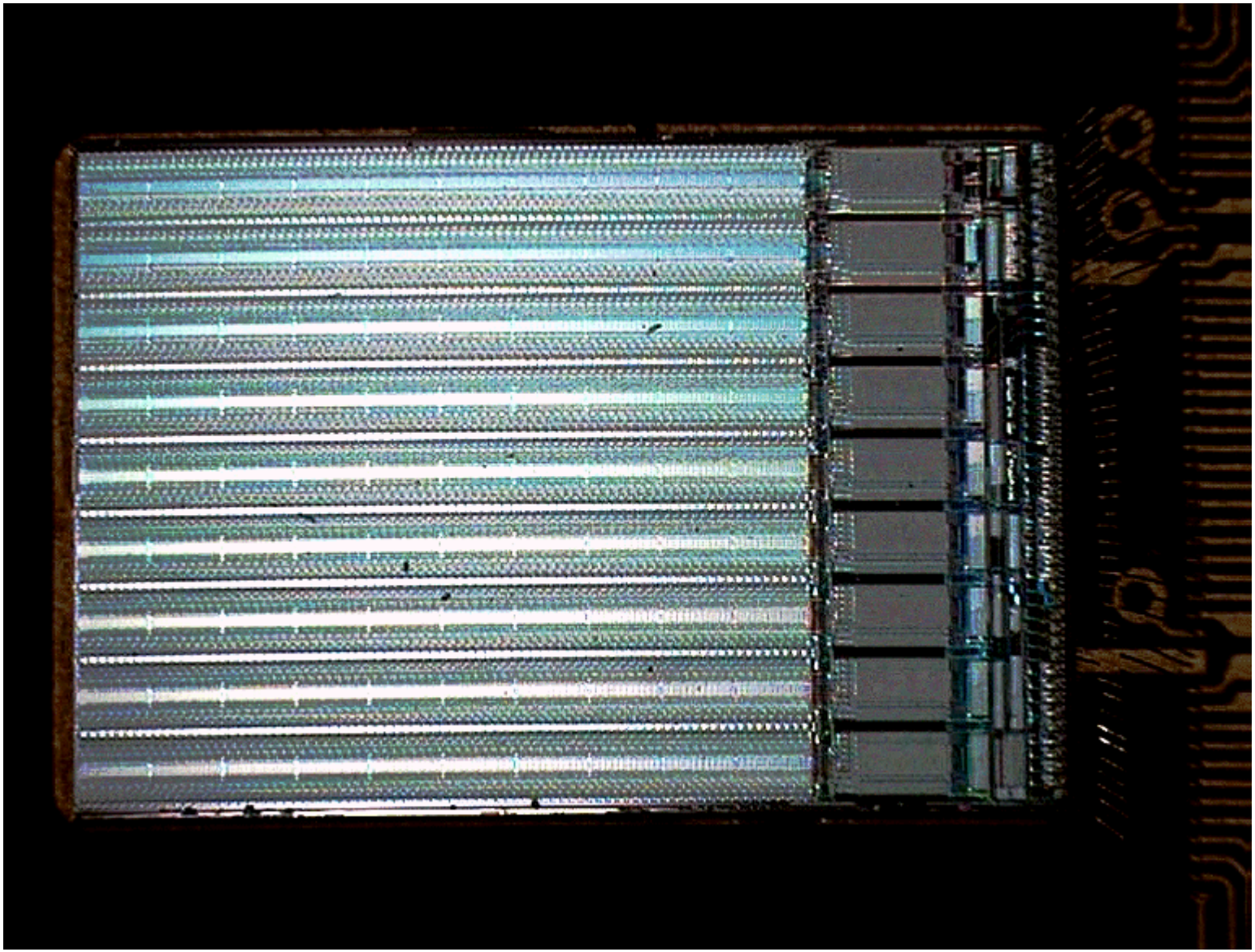
Summary of Recent DMILL Reticle

Reticle included many die (10 in total):

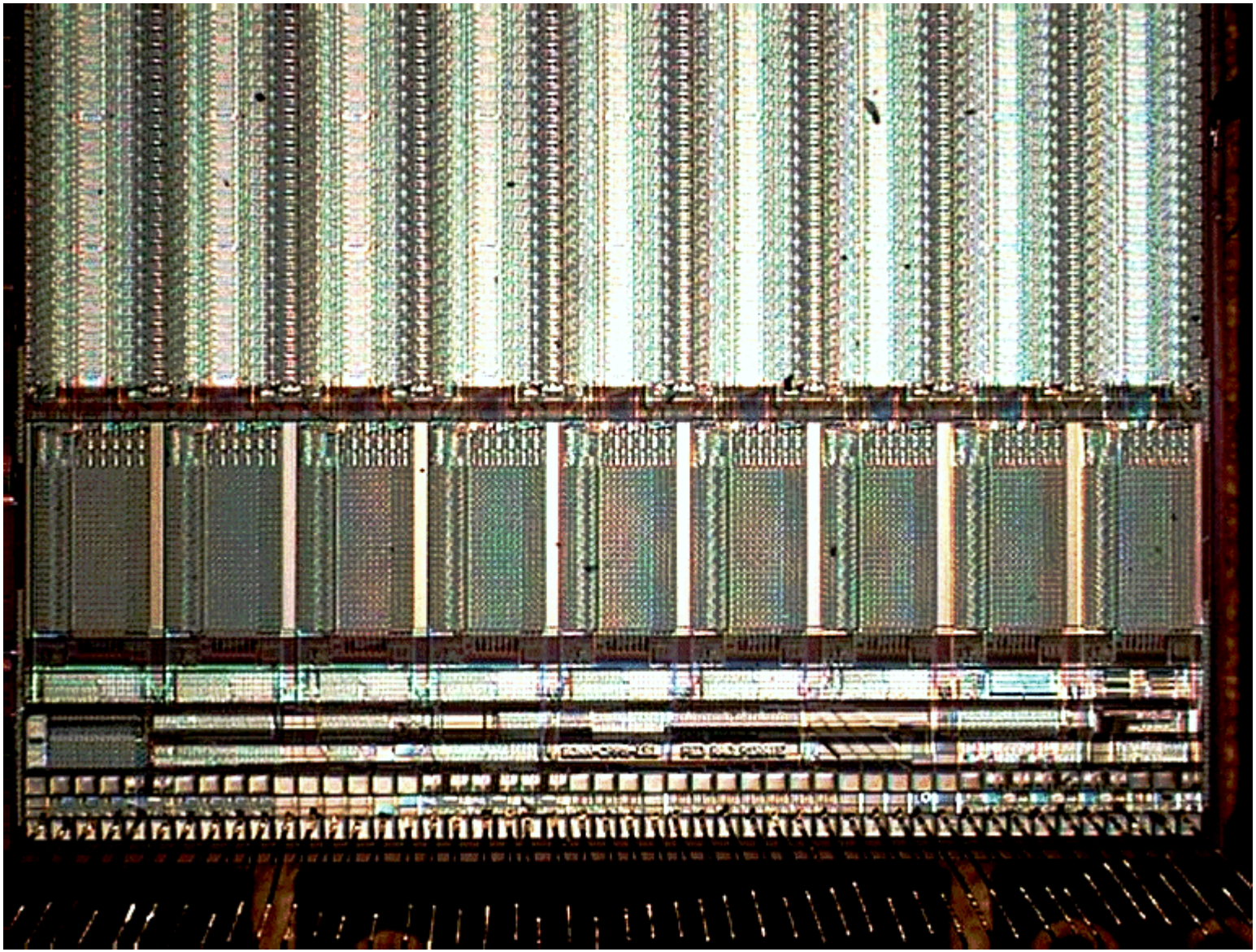
- Two pixel FE chips (FE-D). Present status is that several errors have been found and reproduced in simulation. Several other significant problems are believed to originate in TEMIC fabrication problems
- Prototype MCC chip. A prototype of several key elements of final MCC, about 20mm^2 core size. Includes FIFO block for final chip, plus large synthesized command decoder block. Presently have tested 14 die, of which 11 work. Appear to be no problems with this design, but more complete testing underway.
- Prototype CMOS opto-link chips (one DORIC-p and three VDC-p). VDC seems to work well beyond 100MHz. DORIC has oscillations in biassing circuitry, presently under study. No systems tests including BER yet.
- Additional test chips: LVDS buffer for rad-hard test board, PM bar with W/L arrays and special pixel transistors, Analog Test chip with all critical FE-D analog elements. All work well, and transistor parameter measurements suggest run is slightly faster than typical. Many detailed characterizations of Analog Test Chip.
- Plan to irradiate at least several of the test chips to relevant doses in April in PS.

Testing still continuing...

FE-D Chip under test:



Details of Bottom of Chip:



What works in FE-D:

Answer: Almost everything works from the design point of view:

- Studies of analog blocks, including current reference, current and voltage DACs, internal calibration circuit, etc. indicate all behave well, with exception of one layout error.
- Analog performance is very close to what we expect in terms of shaping time, noise and threshold dispersion, timewalk performance, charge measurements, etc. Performance not yet confirmed with bump-bonded assemblies - delivery of single chips from both bumping vendors expected within 2 weeks. Many system level measurements now made, as well as individual blocks. Some systematic effects seen and under study (e.g. TOT charge calibration has large left-right variation).
- Digital readout works well, including data transfer from column pairs at 20 MHz, with signal recovery at bottom of column by sense amplifiers. Data transfered from chip is correct under almost all circumstances. Major problem is high VDD required for correct operation. This is now understood to be a buffering error.
- Power consumption of many blocks studied for DC and as a function of XCK frequency. For some chips, the agreement with expectations is very good.

Summary of FE-D Design Errors

Analog:

- VTH amplifier layout error (mistake not caught due to design kit error). Presently fixed by FIB surgery.

Integration:

- Basic problem: Missing or mis-sized buffers in several critical locations. Clearly, we are reviewing buffer sizing in detail for the entire chip.
- Several buffers for control logic were undersized, so some commands must be “slowed down” in software.
- Two critical clocks (XCK, CLK1/CLK2) not distributed with adequate buffering, but simulations and measurements indicate these errors are dangerous but not fatal in pre-rad chip operation.
- Missing buffer in serial output stream. This causes data corruption unless VDD supply increased to maximum value permitted by process (about 5V). Have verified using FIB surgery that bringing this signal out directly using an active probe allows us to operate the full chip correctly with VDD = 3.0V. Simulations suggest design kit parasitics should be increased by up to 50%.
- Missing connection to one address pad. Mistake not caught due to design kit error.

Digital Readout:

- Missing column masking on Buffer Overflow OR tree.

Serious problems not attributed to design errors:

- Very poor yield on Pixel Register (2880 bit register in pixel matrix used for individual pixel control).
- Note this register is “quasi-static” in order to reduce transistor count. Extensive analysis examined behavior of defective pixels as a function of VDD, clock frequency and duty cycle, and made detailed comparisons with simulations. Yield is about 0.3 for 3mm^2 of circuitry. Very good consistency with a model in which a particular PMOS has a defect rate of 1:5000, with the defect being a drain-source resistance of several megohms.
- Defective pixels which cause peculiar digital “oscillations” in the column-pair readout circuitry. Detailed studies of behavior, and comparisons with simulations, suggest a problem with a defective NMOS, also with a drain-source resistance of several megohms. Here, the defect rate is much higher, about 1:200.
- Significant number of chips with anomalous digital power consumption.
- Result is that our yield for chips which pass even simple digital checks is essentially zero (very similar chip in rad-soft process had 92% yield over 20 wafers, with much more sophisticated testing).

Work in Progress for FE-D

- Work on measuring defective MOS using FIB modifications, and proving they are not design faults. Bonn has recently measured an NMOS in the readout logic to have off-resistance of 250KΩ, and very peculiar sub-threshold behavior. LBL has added gate and drain pads to 10 devices and will test them soon.
- Two wafers sent out for bump-bonding. Test assemblies as soon as they return (may require surgery on some to make SDO mod to allow 3.0V VDD operation).
- Provide GDS for TEMIC backup run (4 new wafers, already processed to poly with existing FE-D masks, we can change M1/M2). Have implemented small pads over all critical SR and Readout dynamic nodes, and cut traces for VTH circuit. This run should take 4-6 weeks to return. We will wait for these wafers, and quickly characterize them, before sending in FE-D2.
- Complete presently known modifications to FE-D design database to make FE-D2. List of changes is quite modest (but critical !). Continue intensive simulation and verification work on FE-D2 database.
- Do PS irradiations on PM bars and Analog Test chips to validate performance of individual devices and analog portions of FE-D under irradiation.
- Actual submission date for FE-D2 will depend on factors above, but should be as early as possible (April) to allow us to complete serious evaluation this Summer (PS and other irradiations, single-chip and module assemblies, testbeams, etc.). However, little reason to submit if there are no clear improvements from TEMIC.

Summary of Status of FE-H (Honeywell version)

- Infrastructure work now done (Standard Cell library, Cadence files, etc.), and last concerns about completeness of “new” Layout Rules scheme now seem to be resolved.
- Transfer agreements with collaborators “essentially” in place. Honeywell has finally shipped relevant documentation so Bonn and Marseille can begin design contributions. However, they are almost fully engaged by DMILL work.
- First significant work on layout indicates we can improve on several aspects of FE-D, while achieving a smaller pixel size. This is due to smaller device size and closer packing, plus third metal layer. Presently simulating column pair (without EOC buffering), using improved hit logic, RAM cell, and sense amplifiers.
- Effort is presently significantly reduced due to activity in understanding FE-D and submitting FE-D2. This is certainly generating delay. Bonn is not yet contributing at all, and CPPM is very slowly beginning work on the analog front-end. Have just added a thrid engineer to the LBL team (and he has considerable experience with FE-D already). Hope to submit design for engineering run by August 00.
- This would provide first chips by the end of 2000.

Radiation Hardness Testing:

- **Characterization of processes using single devices and test structures:** This work has been carried out already for both DMILL and HSOI. The DMILL work was done when the process was still under development with LETI.
- **Irradiate complete circuit blocks from present designs:** An example is the analog test chip created for the FE-D run. It allows full studies of the front-end, including adding capacitive loads and leakage current, in a small simple chip.
- **Irradiate FE chips while they are operating:** Have already built "rad-hard test board" for this purpose. Constructing an optimized "parametric" tester to characterize chips in detail (essentially use commercial ATE chips to build a custom IC tester). This allows changing clock frequencies, scanning phasing/ timing, and scanning I/O thresholds/voltages to evaluate how much margin a given die has for achieving its operational specifications. This electronics is being developed at LBL, and should be ready in about 4 months.
- This is the technique we propose to use for selecting "known good die". These die should remain good (with high confidence level) after irradiation. The actual production cuts would have to be "tuned" by characterizing many chips both before and after irradiation. Wafer probe cuts should be optimized to provide acceptable yield before irradiation, as well as good confidence level of continued operation after irradiation.

US Roles:

- **Overall Electronics coordination:** I have been overall electronics coordinator for pixels since 1998.
- **FE-D design effort:** Our contributions were the digital readout design. The design team was two full-time designers plus myself. Both designers left during 1999. One is returning and will be part of FE-H design team. We also play a major role in testing, including frequent trips to our FIB vendor.
- **FE-H design effort:** Up to now, we are the only real HEP users of this process. We developed a complete front-end design (prototyped in Nov. 98), and characterized the process pre-rad and post-rad. Our present design team consists of two IC designers, with a third being added this week. Our roles are digital readout and overall integration, with Bonn contributing some analog blocks, and CPPM providing the front-end design.
- **DORIC-p/VDC-p design effort:** OSU has one engineer and one postdoc part-time, plus part of a senior physicist. They are working on design and testing.
- **Testing systems:** LBL (initially in collaboration with Wisconsin) developed the first generation test system (VME-based PLL module, PCC board, and single-chip support boards). We are presently designing a second generation test system, which includes greater capability for testing at different XCK frequencies. We will also develop a “burn-in” board to allow continuous operation of up to 16 modules with periodic sampling of their performance.

Remaining Issues:

Critical issue:

- Successful fabrication of rad-hard versions of on-detector electronics. First run with TEMIC did not produce viable chips.
- Given the large number of die required, the yield must reach some acceptable level. Lower yield requires more wafers to purchase and probe, and also process through bump-deposition.

Resources:

- Our IC design resources are stretched to the limit by the present activity. The long design period also requires us to cope with very extensive turn-over in design teams. This is exacerbated by present problems with fabrication which require large diversions of expert resources into very low level debugging.

Other Major Issue:

- Have not yet produced enough fully functioning modules to properly evaluate and validate system design.
- Present concerns include: demonstrating radiation hardness of module including all components, and measuring noise and pickup sensitivity with real power cables and power supplies

Some "what ifs":

Scenario 1: DMILL fails:

- After further investigations and another iteration, TEMIC could still fail to fabricate FE-D with the yield and radiation hardness needed for ATLAS.
- In our present schedule, this "no go" point should be reached about Sept 00. The procedure that we have agreed to involves one further engineering run (FE-D2). This run is contingent on TEMIC and ATLAS reaching some understanding which would give a reasonable probability of significantly improved results over FE-D1 run. What is difficult to define is when we have made every appropriate effort for this next run to succeed, and when it is time to switch vendors.
- In this case, we would effectively switch to HSOI as our backup. The delay incurred in this case would depend on how successful our first FE-H run is, but would not be less than six months.

Scenario 2: Neither DMILL nor HSOI look likely to succeed:

- Backup in this case is commercial deep sub-micron process with modified layout rules (IBM or TSMC 0.25μ). Delays would be substantial - at least 12 months.
- We are beginning to look seriously at this, and are establishing NDA's with our FE design institutes. We are exploring collaboration with experienced groups (CERN and RAL), but little significant work is likely before the end of 2000.

Deep Sub-micron Approach:

- One of dominant effects of irradiation of CMOS devices is creation of trapped charge in the critical gate oxide layers. Below about 10nm oxide thickness, the charge trapping largely vanishes due to quantum tunneling effects. Modern 0.25µ processes are the first to operate fully in this regime (they have 5-6nm oxides).
- The RD-49 collaboration has studied details, confirming that if one controls leakage paths using layout, then a commercial 0.25µ process can be very rad-hard (circuits tested to 30MRad). Many technical concerns addressed, but basically no experience with full-scale devices, so still a risky path.
- Little experience with analog designs, so some prototyping would most likely be needed. This would introduce additional delays in transferring our designs.
- CERN has negotiated a frame contract for LHC with IBM for their CMOS6 process. The price is significantly lower than the traditional rad-hard vendors (could expect a cost reduction of factor 5 or possibly more).
- This places us into a commercial mainstream, where we can be assured of low prices and availability in the future. Eventually, pixels will pursue this path for B-layer upgrades, and perhaps even to address “lifetime buy” issues for spares.
- We are presently extremely short of manpower for our baseline approaches (FE-D and FE-H), particularly in the area of analog design, where first effort would be needed. We cannot divert any significant effort to this until the end of 2000.

Deliverables:

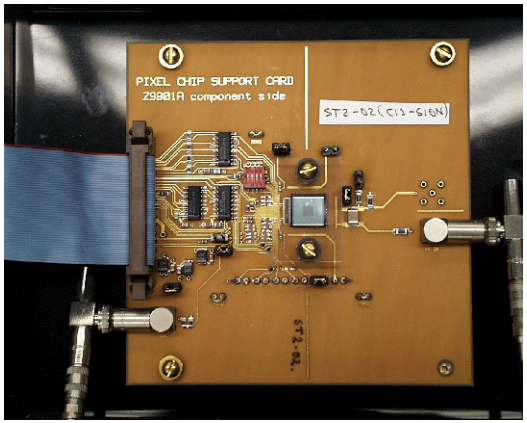
US Responsibilities include:

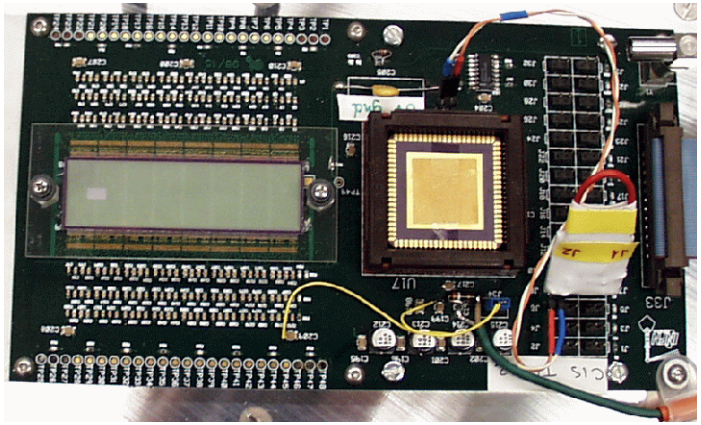
- FE chip design, testing and production (LBL): Contribute roughly 20% towards the common procurement of the series production. Estimate below is based on about 1300 TEMIC wafers for outer layers (30% die yield, plus module assembly yield).
- Opto-link chip design, testing and production (OSU): Contribute approximately 50% towards the common procurement of the series production. However, the die sizes are small and this is a tiny procurement (single lot engineering run).
- Design and provide hardware/software for lab/testbeam single chip and module testing, production FE wafer probing, production module testing/burn-in (LBL).
- Present US Production Cost Estimate (preliminary) is:

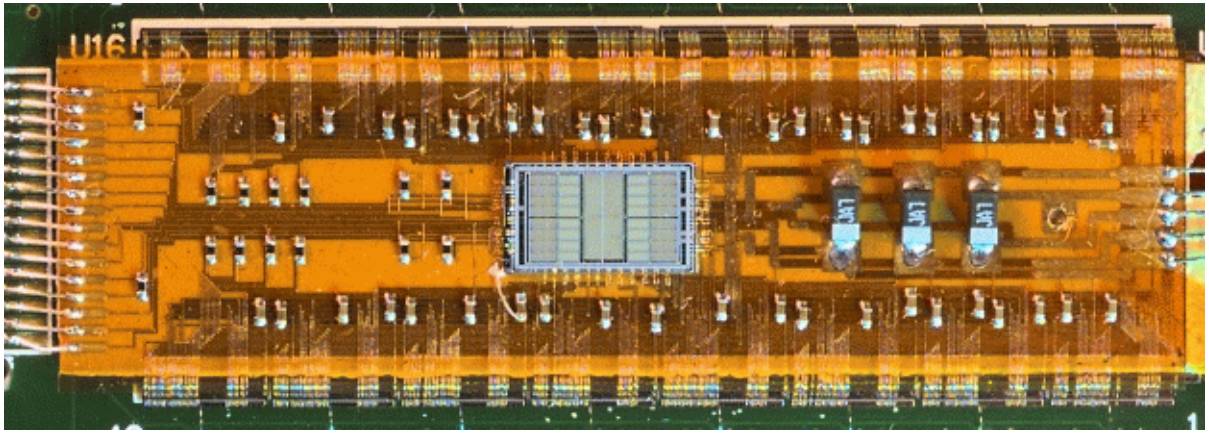
WBS Number	Description	Base Cost	Cont Cost (k$)	Cont %	Total Cost	EDIA Labor	Mfg Labor	EDIA Matls	Mfg Matls	FTEs Project	FTEs Other
1.1.1.3.3	Production	2125	1588	75	3712	0	73	0	2052	2.0	0.0
1.1.1.3.3.1	Front-end ICs	2027	1576	78	3603	0	67	0	1959	1.7	0.0
1.1.1.3.3.1.1	Layers 1/2 and Disks	1483	1380	93	2863	0	0	0	1483	0.0	0.0
1.1.1.3.3.1.2	B-layer	463	177	38	640	0	0	0	463	0.0	0.0
1.1.1.3.3.1.3	Testing	81	19	24	100	0	67	0	13	1.7	0.0
1.1.1.3.3.2	Optoelectronics	98	12	12	110	0	6	0	93	0.3	0.0
1.1.1.3.3.2.1	Preproduction	0	0	0	0	0	0	0	0	0.0	0.0
1.1.1.3.3.2.2	Production	66	0	0	66	0	0	0	66	0.0	0.0
1.1.1.3.3.2.3	Testing	32	12	36	44	0	6	0	27	0.3	0.0

Module Prototyping:

- Built many “single chip” devices using smaller sensors for small-scale studies. Some studies were done with irradiated sensors and rad-soft electronics.
- Built about 10 modules with IZM solder bumps, several as “bare” modules with interconnections on PC board, several as “Flex” modules, others as “MCM-D” modules. Some, but not all, of these modules work very well.



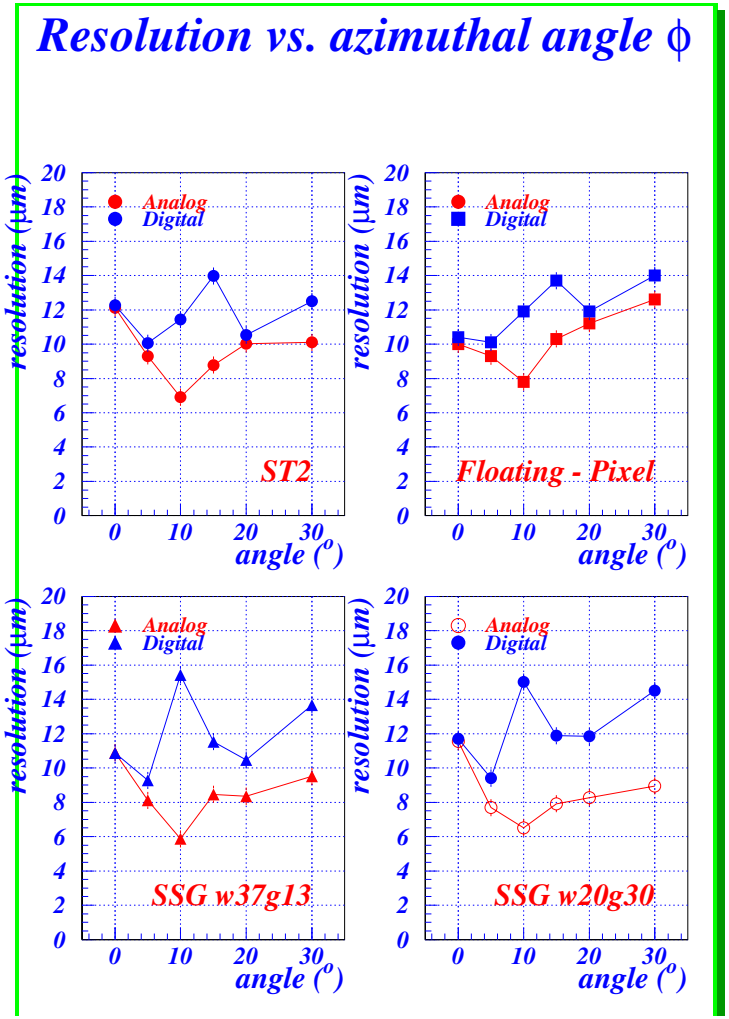


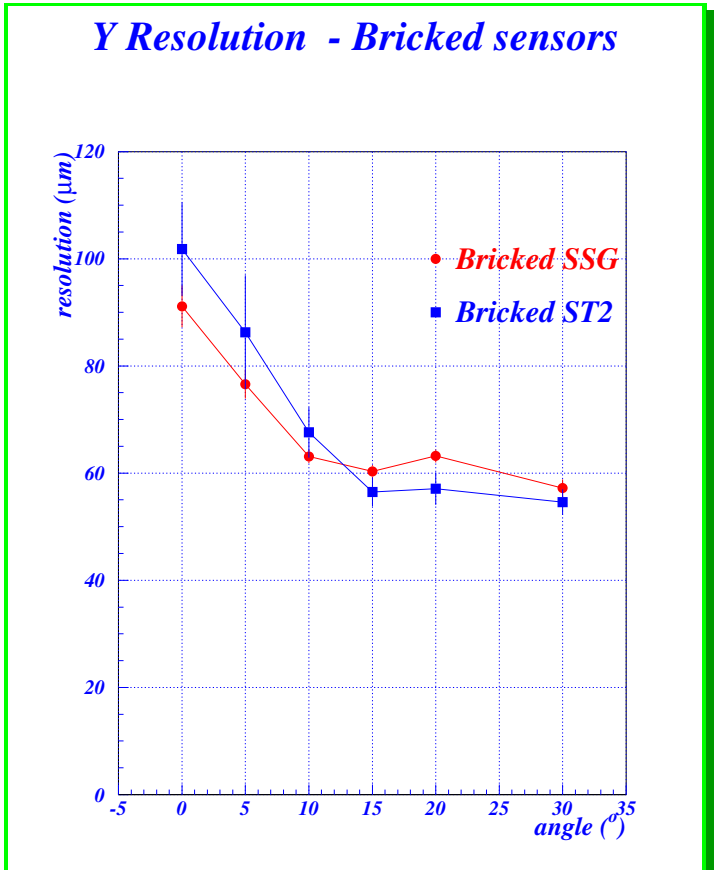


Electronics/Sensor Prototype Results

Measure resolution versus incident track angle:

- Compare digital (binary) and analog algorithms for different sensor types, and also compare effect of "bricking" (half-pixel stagger) in long direction of pixel:



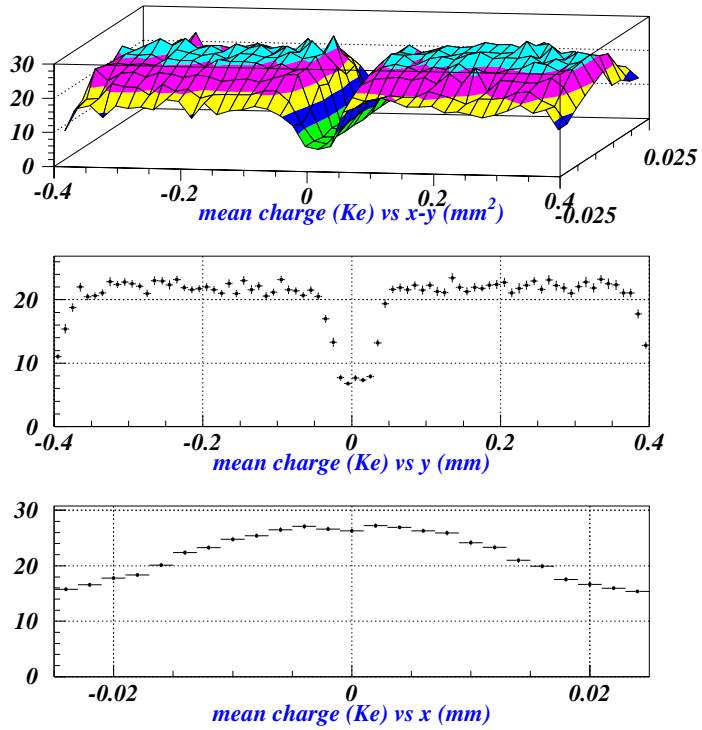


Could achieve perhaps 8-10μ in narrow and 60-80μ in wide direction for best case in barrel

Measure charge collection versus track location in pixel:

- Original n-ring design has serious charge loss problems, while new small-gap design is much better, with only small loss at bias dot location:

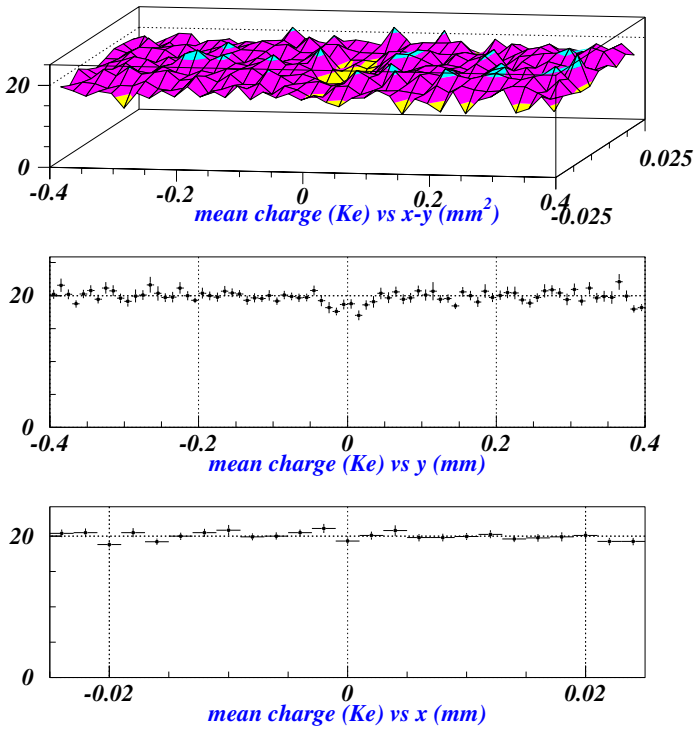
Tile 2 Design Threshold 2 Ke



large loss (0.7) near the grid
loss located ± 30 μm around the grid
losses at the pixel edges

Design 1.b:

- *p-spray insulation*
- *no floating atoll*
- *modified bias grid*



Measure efficiency as a function of track arrival time:

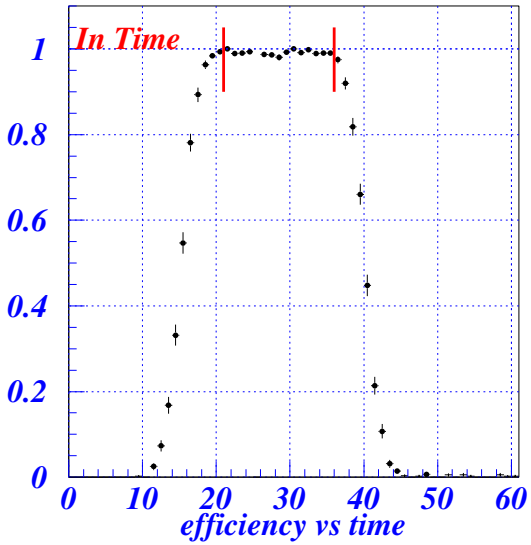
- Behavior of new design (pre-rad) is excellent, and behavior of old design (post-rad) is very good, provided that poor charge collection regions are removed:

Efficiency 'In Time'

Detector Tile 2 new design (with bias grid)

not Irradiated - Thr. 3 Ke

efficiency 99.1		***Losses***	***0.9***
1 hit	***81.8***	***0 hits***	***0.4***
2 hits	***15.6***	***not matched***	***0.1***
>2 hits	***1.7***	***not in time***	***0.4***

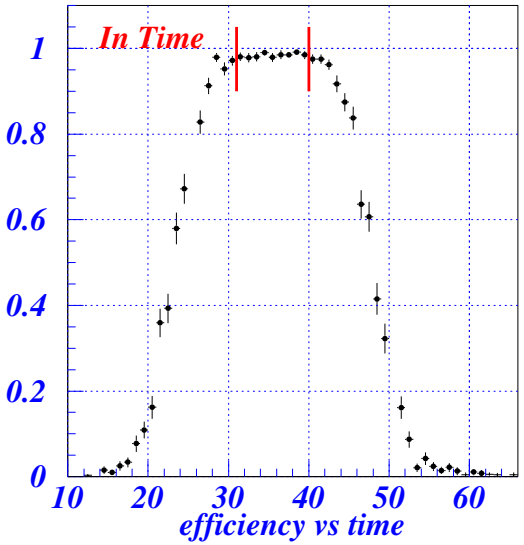


Efficiency 'In Time'

Detector Tile 2 - Irradiated V_{bias} = 600 V

Fluence 10^{15} n/cm^2 - Thr. 3 Ke

efficiency 98.4		***Losses***	***1.6***
1 hit	***94.2***	***0 hits***	***0.4***
2 hits	***3.1***	***not matched***	***0.0***
>2 hits	***1.1***	***not in time***	***1.2***



|xloc| < 0.01

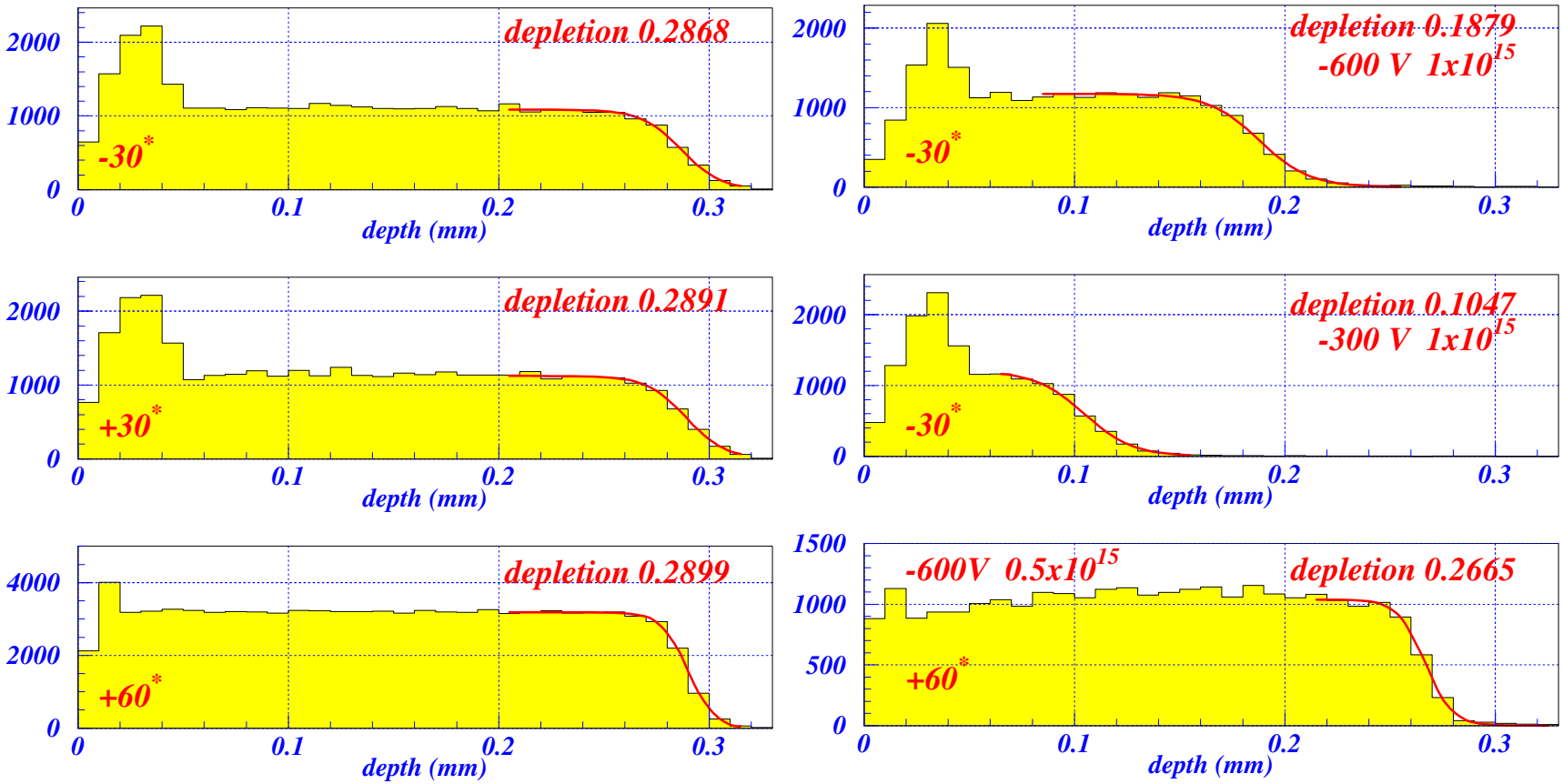
|yloc| < 0.15

Measure depletion depth in sensors:

- Look at cluster width for highly inclined tracks and use this to measure uniformity and depth of charge collection inside of sensor:

Not irradiated - depletion depth

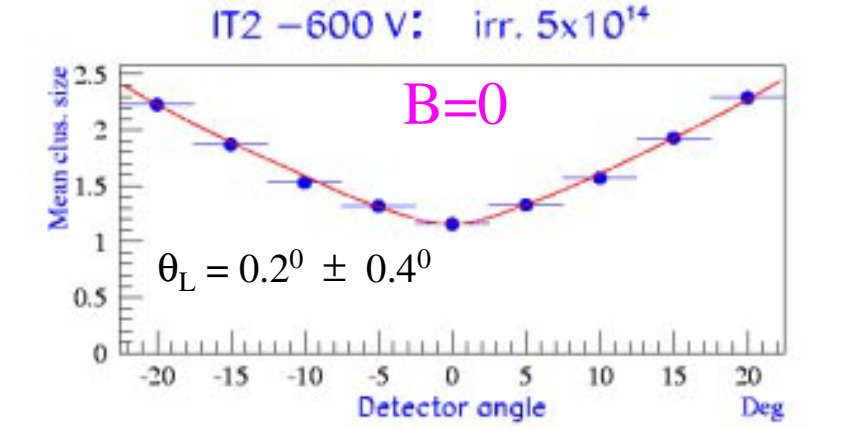
Irradiated - depletion depth



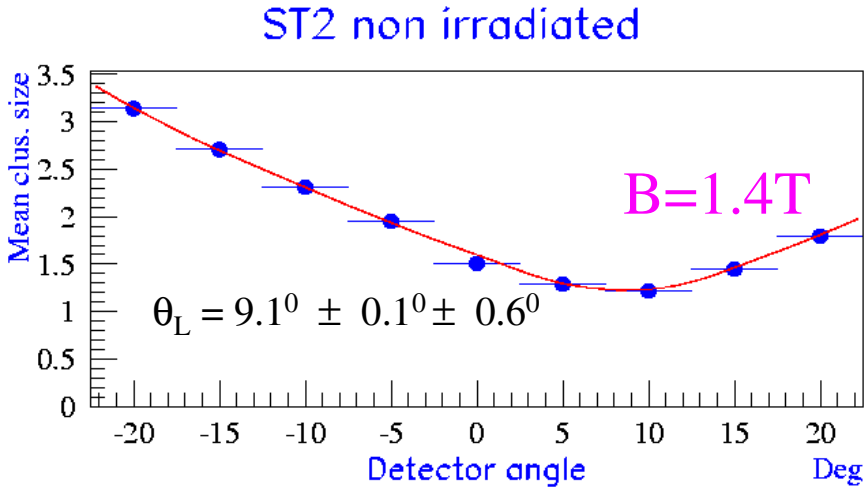
- Pre-rad result agrees with 280μ thickness. At 600V bias, lose full depletion at about half the lifetime dose, and still collect from about 180μ after lifetime dose.

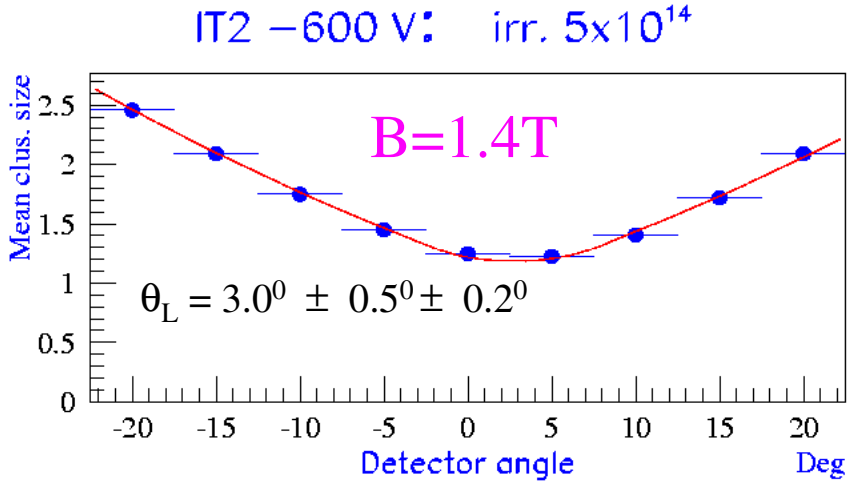
Measure Lorentz angle in sensors:

- Use cluster width versus angle of incidence, doing parallel runs with and without magnetic field, to extract angle at which cluster width is minimum:



not irradiated	**$9.1^0 \pm 0.1^0 \pm 0.6^0$**
dose 5 10^{14} n/cm^2	**$3.0^0 \pm 0.5^0 \pm 0.2^0$**
dose 10^{15} n/cm^2	**$3.2^0 \pm 1.2^0 \pm 0.5^0$**





- Significant reduction after irradiation due to reduced mobility at higher E fields ?

Summary and Conclusions

Sensors:

- Extensive design and prototype program essentially complete. Prototype performance, including operation after lifetime radiation doses, is acceptable.
- Oxygenated material appears to provide significant increase in operating margins (lifetime dose and access scenarios).
- Sensor FDR and PRR completed, Tender in progress.
- Additional radiation testing of final design will be performed before launching pre-production in the middle of this calendar year.

Electronics:

- Prototypes built using rad-soft electronics have been extensively tested in lab and testbeam, Present designs basically meet all ATLAS requirements.
- Design of first rad-hard prototype in DMILL appears sound, but yield is unacceptably low. Working with vendor to understand problems. Backup run to allow better diagnostics is in progress, and pending improved understanding, a new engineering run could occur within 4-6 weeks.
- Expect that go/no-go decision on whether to continue with TEMIC could be made by September this year.

- Work on Honeywell version of design proceeding more slowly than expected, due to problems with DMILL version. If only used for B-layer, schedule is acceptable.
- Deep sub-micron approach is attractive, but we cannot contemplate diverting any significant effort from our ongoing DMILL and Honeywell efforts this year.